WHAT IS CLAIMED IS:

1. A power MOSFET comprising:

a drain layer of a first conductivity type;

a drift layer of the first conductivity type provided on said drain layer;

a base layer of a second conductivity type provided on said drift layer;

a source region of the first conductivity type provided on said base layer;

a gate insulating film formed on an inner wall surface of a trench penetrating the base layer and reaching at said drift layer; and

a gate electrode provided on said gate insulating film inside said trench, wherein

said gate insulating film is formed such that a portion thereof adjacent to said drift layer is thicker than a portion thereof adjacent to said base layer, and said drift layer has an impurity concentration gradient higher in the vicinity of said drain layer and lower in the vicinity of said source region along a depth direction of the trench.

2. The power MOSFET according to claim 1, wherein the impurity concentration of said drift layer is in the range between 1×10^{16} and $9 \times 10^{16}/cm^3$, in the portion adjacent to base layer, and is in the range between 1×10^{17} and $3 \times 10^{17}/cm^3$ in a portion adjacent to the drain layer.

3. The power MOSFET according to claim 1, wherein said drift layer has a portion in which the impurity concentration of said first conductivity type along a depth direction of the trench is the minimum.

4. The power MOSFET according to claim 3, wherein the impurity concentration of said drift layer is in the range between 1×10^{17} and $3 \times 10^{17}/cm^3$, in the portion adjacent to said base layer, and is in the range between 1×10^{16} and $9 \times 10^{16}/cm^3$ in the portion having the minimum concentration, and is in the range between 1×10^{17} and $3 \times 10^{17}/cm^3$ in a portion adjacent to said drain layer.

5. The power MOSFET according to claim 1, wherein a width of said base layer disposed between a pair of the gate insulating films adjacent to each other is equal to or less than 0.5 μm.

6. The power MOSFET according to claim 2, wherein a width of said base layer disposed between a pair of the gate insulating films adjacent to each other is equal to or less than 0.5 μm.

7. The power MOSFET according to claim 3, wherein a width of said base layer disposed between a pair of the gate insulating films adjacent to each other is equal to or less than 0.5 μm.

8. The power MOSFET according to claim 4, wherein a width of said base layer disposed between a pair of the gate insulating films adjacent to each other is

equal to or less than 0.5 μm.

9. The power MOSFET according to claim 1, wherein said gate insulating film reaches at said drain layer.

10. The power MOSFET according to claim 2, wherein said gate insulating film reaches at said drain layer.

11. The power MOSFET according to claim 3, wherein said gate insulating film reaches at said drain layer.

12. The power MOSFET according to claim 4, wherein said gate insulating film reaches at said drain layer.

13. The power MOSFET according to claim 1, wherein said gate insulating film has portions facing said base layer with similar thickness, and portions facing said drift layer with similar thickness.

14. The power MOSFET according to claim 1, wherein said gate insulating film has portions facing said base layer with similar thickness, and portions facing said drift layer with a thickness increasing from said base layer to said drain layer.

15. The power MOSFET according to claim 1, wherein said gate insulating film has portions facing said base layer with similar thickness, and portions facing said drift layer with a thickness increasing in a step like fashion from said base layer to said drain layer.

16. A power MOSFET comprising:

a drain layer of a first conductivity type;

a drift layer of the first conductivity type provided on said drain layer;

a base layer of the first conductivity type provided on said drift layer;

a source region of the first conductivity type provided on said base layer;

a gate insulating film formed on an inner wall surface of a trench penetrating the base layer and reaching at said drift layer; and

a gate electrode provided on said gate insulating film inside said trench, wherein

said gate insulating film is formed such that a portion thereof adjacent to said drift layer is thicker than a portion thereof adjacent to said base layer, and said drift layer has an impurity concentration gradient higher in the vicinity of said drain layer and lower in the vicinity of said source region along a depth direction of the trench.

17. The power MOSFET according to claim 16, wherein the impurity concentration of said drift layer is in the range between 1×10^{16} and $9 \times 10^{16}/cm^3$, in the portion adjacent to said base layer, and is in the range between 1×10^{17} and $3 \times 10^{17}/cm^3$ in a portion adjacent to said drain layer.

18. The power MOSFET according to claim 16, wherein said drift layer has a portion in which the impurity concentration of said first conductivity type along a depth direction of the trench is the minimum.

19. The power MOSFET according to claim 18,

wherein the impurity concentration of said drift layer is in the range between 1×10^{17} and $3 \times 10^{17}/cm^3$, in the portion adjacent to said base layer, and is in the range between 1×10^{16} and $9 \times 10^{16}/cm^3$ in the portion having the minimum concentration, and is in the range between 1×10^{17} and $3 \times 10^{17}/cm^3$ in a portion adjacent to said drain layer.

20. The power MOSFET according to claim 16, wherein a width of said base layer disposed between a pair of the gate insulating films adjacent to each other is equal to or less than 0.5 µm.

21. The power MOSFET according to claim 17, wherein a width of said base layer disposed between a pair of the gate insulating films adjacent to each other is equal to or less than 0.5 µm.

22. The power MOSFET according to claim 18, wherein a width of said base layer disposed between a pair of the gate insulating films adjacent to each other is equal to or less than 0.5 µm.

23. The power MOSFET according to claim 19, wherein a width of said base layer disposed between a pair of the gate insulating films adjacent to each other is equal to or less than 0.5 µm.

24. The power MOSFET according to claim 16, wherein said gate insulating film reaches at said drain layer.

25. The power MOSFET according to claim 17, wherein said gate insulating film reaches at said drain layer.

26. The power MOSFET according to claim 18, wherein said gate insulating film reaches at said drain layer.

27. The power MOSFET according to claim 19, wherein said gate insulating film reaches at said drain layer.

28. The power MOSFET according to claim 16, wherein said gate insulating film has portions facing said base layer with similar thickness, and portions facing said drift layer with similar thickness.

29. The power MOSFET according to claim 16, wherein said gate insulating film has portions facing said base layer with similar thickness, and portions facing said drift layer with a thickness increasing from said base layer to said drain layer.

30. The power MOSFET according to claim 16, wherein said gate insulating film has portions facing said base layer with similar thickness, and portions facing said drift layer with a thickness increasing in a step like fashion from said base layer to said drain layer.

31. A method of manufacturing a power MOSFET, comprising:

epitaxially growing a drift layer of a first conductivity type on a first conductivity type semiconductor substrate used as a drain layer, said drift layer being doped with impurities having a

concentration distribution increasing up to said semiconductor substrate;

epitaxially growing a base layer of a second conductivity type on said drift layer;

forming a source region of the first conductivity type on said base layer;

forming a trench penetrating said source region and said base layer to reach at said drift layer; and

forming a trenched gate structure including a gate insulating film and a gate electrode, said gate insulating film having a thin portion facing said base layer and a thick portion facing said drift layer.

32. The method of manufacturing a power MOSFET according to claim 31, wherein said forming the drift layer comprises:

forming a first epitaxial layer of the first conductivity type on said semiconductor substrate with a first impurity concentration;

forming a second epitaxial layer of the first conductivity type of said first epitaxial layer with a second impurity concentration lower than that of said first epitaxial layer; and

heat treating said first and second epitaxial layers for smoothing the first and second impurity concentrations.

33. The method of manufacturing a power MOSFET according to claim 32, which further comprises:

implanting impurities from a surface of said second epitaxial layer up to a predetermined depth thereof; and

diffusing the implanted impurities into said second epitaxial layer to form a peak of the impurity concentration in said second epitaxial layer.